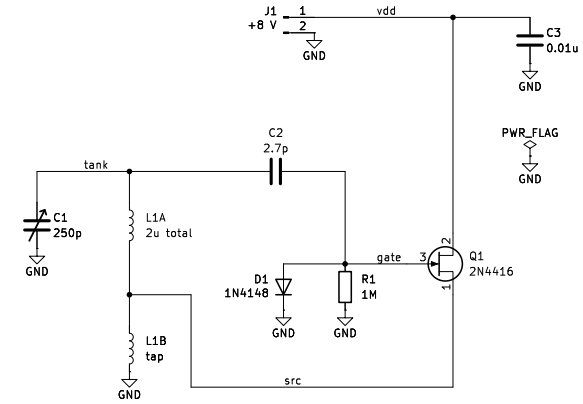
Hartley VFO with 2N4416 JFET

40m · 8 V · sim-pass
EMRFD p. 4.3

A basic tunable LC oscillator (VFO) around one JFET. Turning C1 tunes the frequency.



L1: 2 uH, tapped about 20% of the turns up from ground (EMRFD p. 4.3). C1: 250 pF tuning.

D1 (anode at gate) clamps the gate and sets the operating level.

BUILD LIST: TICK AS YOU GO

	Ref	Value	Qty	Part / notes
☐	C1	250 pF	1	250 pF variable capacitor
☐	C2	2.7 pF	1	
☐	C3	0.01 µF	1	
☐	D1	1N4148	1	1N4148
☐	J1	+8 V	1	
☐	L1	2 µH	1	one part, units L1A (2u total), L1B (tap)
☐	Q1	2N4416	1	2N4416 N-channel JFET
☐	R1	1 MΩ	1	

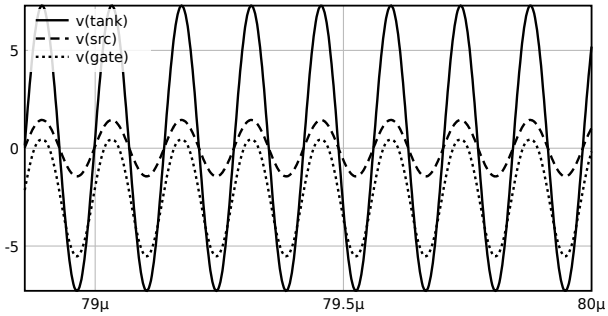
BUILD NOTES

- L1 is a single 2 µH coil with a tap about 20% of the turns from ground. The figure doesn't give a core; use a stable air or iron-powder form.
- Use NP0/C0G or silver-mica capacitors in the tank for stability.
- The figure has no output port. Take output from the source tap through a buffer such as the W7EL buffer amplifier.

Test: Check the frequency with a counter or a receiver. Adjust the turns or add fixed capacitance to put the tuning range where you want it.

CHECK AGAINST

Check	Expect	Basis
Frequency	7.11 MHz ± 0.05	simulated
Tank voltage	14.6 Vpp ± 2.19	simulated



ngspice sim/startup.cir from the schematic netlist (not a measurement)

Full page:
https://qrpedia.com/circuits/oscillators/hartley-vfo-7mhz-jfet/
Interactive sim, KiCad project, netlist and errata.

SPECIFICATIONS (FULL)

Spec	Value	Basis	Reference
Frequency	7.11 MHz ± 0.05	simulated	sim/startup.cir, C1 at 250 pF
Tank voltage	14.6 Vpp ± 2.19	simulated	sim/startup.cir, coil Q 200 assumed

Simulated values are this build's ngspice results (± the build's check tolerance); book and measured values are as published.

HOW IT WORKS

L1, a 2 µH coil tapped about 20% of the turns up from ground (EMRFD p. 4.3), is the Hartley tank. Q1's source drives the tap, so the coil works as an autotransformer that feeds energy back into the tank. The gate is lightly coupled to the top of the tank through 2.7 pF. The 1N4148, anode at the gate, clamps the gate on positive peaks and sets the operating level. $f = 1/(2\pi\sqrt{(LC)})$; with 2 µH and 250 pF that's 7.1 MHz. The simulation agrees: 7.11 MHz (**simulated**).

WHERE IT COMES FROM

The basic Hartley oscillator in Experimental Methods in RF Design, Chapter 4.

SOURCES

- EMRFD Fig 4.4, p. 4.3 (errata: text-only: p. 4.3: delete the word "viable" from a sentence in the middle column. The schematic is unaffected.)