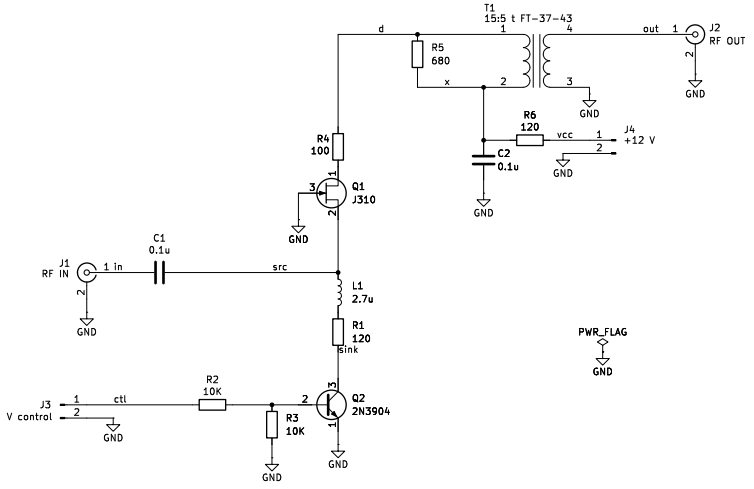
# Common-Gate J310 RF Amplifier



A low-gain, high-intercept RF amplifier for a receiver front end, with good reverse isolation (S12 about −43 dB). It keeps LO leakage off the antenna.




T1: 15 t primary, 5 t secondary on FT−37−43. Bias 12−14 mA from 12 V; V control turns the 2N3904 current sink on.

EMRFD p. 6.12: about 2 dB gain with R5 = 680 ohm (6.5 dB without), OIP3 +28 dBm at 14 MHz, NF 5.0 dB at 21 MHz, S12 −43 dB.

## BUILD LIST: TICK AS YOU GO

| | Ref | Value | Qty | Part / notes |
|---|---|---|---|---|
| ☐ | C1, C2 | 0.1 µF | 2 | |
| ☐ | J1 | RF IN | 1 | |
| ☐ | J2 | RF OUT | 1 | |
| ☐ | J3 | V control | 1 | |
| ☐ | J4 | +12 V | 1 | |
| ☐ | L1 | 2.7 µH | 1 | |
| ☐ | Q1 | J310 | 1 | J310 N-channel JFET |
| ☐ | Q2 | 2N3904 | 1 | |
| ☐ | R1, R6 | 120 Ω | 2 | |
| ☐ | R2, R3 | 10 kΩ | 2 | |
| ☐ | R4 | 100 Ω | 1 | |
| ☐ | R5 | 680 Ω | 1 | 680 ohm |
| ☐ | T1 | 15:5 t FT-37-43 | 1 | FT-37-43 toroid; 15:5 t on FT-37-43 |

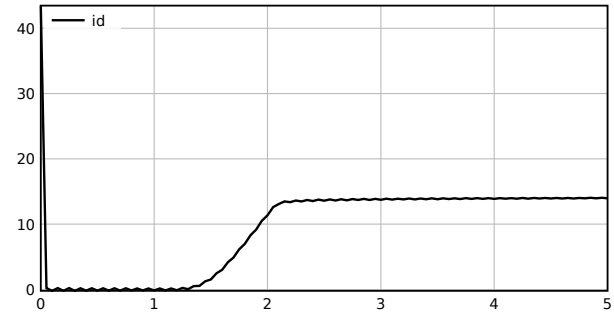
## BUILD NOTES

- Check the J310 pinout against your part's datasheet; the schematic pinout is unverified.
- Adjust the control voltage for 12–14 mA drain current.

**Test:** Measure drain current first. Then check gain and return loss with a signal generator and a return-loss bridge.

## CHECK AGAINST

| Check | Expect | Basis |
|---|---|---|
| Gain | 2 dB | book |
| Output IP3 at 14 MHz | 28 dBm | book |
| Noise figure at 21 MHz | 5 dB | book |
| Reverse isolation S12 | -43 dB | book |
| Gain at 14 MHz | 2 dB ± 0.7 | simulated |
| Return loss at 14 MHz | 13.9 dB ± 2 | simulated |




ngspice sim/bias.cir from the schematic netlist (not a measurement)

**Full page:** https://qrpedia.com/circuits/rx-front-end/common-gate-j310-rf-amp/
Interactive sim, KiCad project, netlist and errata.

## SPECIFICATIONS (FULL)

| Spec | Value | Basis | Reference |
|---|---|---|---|
| Gain | 2 dB | book | EMRFD p. 6.12, R5 = 680 ohm |
| Output IP3 at 14 MHz | 28 dBm | book | EMRFD p. 6.12 |
| Noise figure at 21 MHz | 5 dB | book | EMRFD p. 6.12 |
| Reverse isolation S12 | -43 dB | book | EMRFD p. 6.12 |
| Gain at 14 MHz | 2 dB ± 0.7 | simulated | sim/gain.cir, Vctl 2.0 V |
| Return loss at 14 MHz | 13.9 dB ± 2 | simulated | sim/gain.cir; book 15 dB |

Simulated values are this build's ngspice results (± the build's check tolerance); book and measured values are as published.

## HOW IT WORKS

The J310 runs common gate, so its source presents a near-50 Ω input. A control voltage sets the drain current; the simulation shows current turning on above about 1.5 V and 13.6 mA at 2.0 V. T1 matches the drain to the 50 Ω output. R5 = 680 Ω loads the output for about 2 dB gain; omit it for about 6.5 dB (EMRFD p. 6.12).

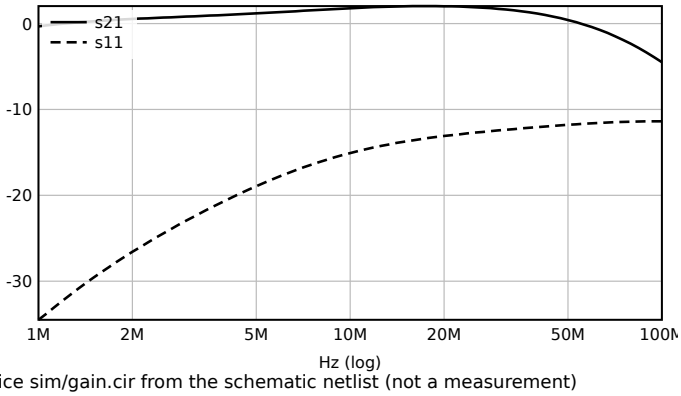
## WHERE IT COMES FROM

A front-end amplifier from Experimental Methods in RF Design, Chapter 6.

## SOURCES

- EMRFD Fig 6.32, p. 6.12

## MORE SIMULATION




ngspice sim/gain.cir from the schematic netlist (not a measurement)